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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/308,032	08/13/1999	BART DIERICKX	16820.P380	5620

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EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/308,032	DIERICKX ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 08/25/2005 have been fully considered but they are not persuasive.

Examiner's response:

2. Applicant argues with regards to claim 3 that Hashimoto et al. does not disclose or suggest an image sensor having "all the pixels of one column of the array being connected to at least one common pixel output line". **The Examiner respectfully disagrees**. Figure 16A shows one pixel (e.g. pixel S1) in each column (e.g. column one), each column being connected to one common output line. This is for illustrative purposes only (i.e. for pixels arranged in a line). Figures 5, 7 and 9 clearly show more than one pixel in each column (The whole array is arranged in a matrix form), wherein each column is being connected to one common output line.

3. Applicant further argues that "col. 20 lines 41-43 which discloses that the switches SW1 to SWn respectively receive sensor signals S1 to Sn from photosensors S1 to Sn arranged in a line or a matrix form." In particular, this passage of Hashimoto discloses that even if a matrix is used, the number of switches equals the number of photosensors, i.e., there are no common column lines with which a switch would be shared among several photosensors. In the implementation illustrated by Figure 16A of Hashimoto, the photosensors are arranged in line form. However, if they would be arranged in matrix form, then Hashimoto teaches having one switch SWj for every photosensor Sj, i.e., having as many switches as there are photosensors. **The Examiner respectfully disagrees. Figure 5 illustrates essentially the same kind of switch SW1 (SW1 comprises transistors labeled as 36-1, 36-2, 37-1, 37-3) as shown in figure 18 and wherein each column comprising more than one pixel per column is connected to**

only one switch (SW1). As such for each common column a switch is shared among several photosensors. Therefore as shown in figure 16a and 18 and as suggested by Hashimoto in column 20 lines 41-43 the switches SW1 to SWn respectively receive sensor signals S1 to Sn from photosensors S1 to Sn arranged in a line or a **matrix form.**

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by (USPN 5,311,320 to Hashimoto).

In regards to claim 3 Hashimoto discloses an image sensor comprising an array of columns and rows of pixels (e.g., column 20, lines 42-43 wherein Hashimoto discloses the pixels are arranged in a matrix form, or array), all of the pixels of one column of the array being connected to at least one common pixel output line (e.g., Fig. 16A, wherein each column would have a common pixel output line in the matrix form as would be recognized by one skilled in the art at the time of the invention) having at least one memory element (e.g., element E of Fig. 16A; column 22, lines 14-38; elements C11 and C12 of Fig. 18) and at least one column output amplifier (e.g., elements A1 – An of Fig. 16A), each common pixel output line being divided through switches (e.g., elements 301A and 303A of Fig. 18) into at least two parallel circuits having said memory element (e.g., Fig. 18), the two parallel circuit being connected through a switch (e.g., elements 302A and 304A of Fig. 18) with the same input of said column amplifying

element (e.g., the output of transistors 302A and 304A goes to the column amplifier element A1 as shown in Fig. 18), said column amplifying elements and the common output amplifier (e.g., element 14A of Fig. 16A) being connected by a single bus (e.g., element 101A of Fig. 16A, wherein there is further a switch between said column amplifying element and said bus (e.g., elements T1 – TN of Fig. 16A), and wherein the image sensor is a CMOS or MOS device (e.g., Figs. 16A and 18).

In regards to claim 4 Hashimoto discloses an image sensor as recited in claim 3, wherein both circuits have memory elements (e.g., elements C11 and C12 of Fig. 18).

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
January 15, 2006

DAVID OMETZ
SUPERVISORY PATENT EXAMINER